

Characterization of a CMOS SPAD sensor designed for fluorescence lifetime spectroscopy

Michele Benetti, Marina Popleteeva, Gian-Franco
Dalla Betta

DISI, Dep. Information Engineering and Computer Science
University of Trento
via Sommarive 14, Povo (TN), Italy
benetti@disi.unitn.it

Lucio Pancheri, David Stoppa

SOI, Smart Optical Sensors and Interfaces
Fondazione Bruno Kessler
via Sommarive 18, Povo (TN), Italy

Abstract—The characterization of a 10x10-SPAD detector module fabricated in a 0.35 μ m High Voltage CMOS technology is presented. The detector is designed to find application in Fluorescence Lifetime spectroscopy and is capable of performing lifetime measurement by using the time-gated technique. The characterization explores the dark count distribution, the detector dynamic range and the gating performances. More than 70% of single SPADs have a dark count rate lower than 1 kHz at the excess bias voltage of 1.8V and do not exceed 2 kHz at the bias voltage of 4.8V. Exploiting the intrinsic features of the detector a direct measurement of the optical cross talk between neighboring SPAD in the matrix was performed. The cross talk was found to be in the range from 2% to 3% for lateral neighbors, and between 0.3% and 0.5% for diagonal neighbors. A dynamic range exceeding 120 dB was observed with a maximum count rate before saturation of 500 MHz. Time gating resolution was found to be less than 1 ns. A fluorescent lifetime measurement of ZnS-ZnSe quantum-dot reference slides was performed and the non-uniformity of the calculated lifetime value was lower than 1% across the matrix. The application of the detector in the construction of a lifetime acquisition system is analyzed estimating the detector data throughput. External resources needed to build the acquisition system are estimated and the FPGA-based acquisition system used during characterizations is described.

Keywords—Single Photon Avalanche Diode; Fluorescence Lifetime; Time-correlated Fluorescence Spectroscopy; FPGA

I. INTRODUCTION

The combination of Single Photon Avalanche Diode (SPAD) detectors and digital processing electronics in a monolithic CMOS chip offer interesting and mostly unexplored opportunities for the realization of low-cost and user friendly instrumentation [1].

The measurement of the decay time of fluorescent molecules (namely Lifetime spectroscopy), a powerful tool used in a large number of molecular studies, fits well with the logic features that can be realized in CMOS technology, especially if the Lifetime measurement is accomplished following the Time-gated method. This method is well described in [2] and depicted in Fig. 1. In this sketch the Lifetime detector presented in this article, which was realized in 0.35 μ m High Voltage CMOS technology, collects the fluorescent light emission during two subsequent time windows. Using two time windows the device permits the

measure of a fluorescent emission that follows a simple exponential decay. CMOS logic elements were used in the design of the front-end electronics of this device to reduce the effect of the typical noise characteristic of SPADs (the dark count), to extend the detector dynamic range and to reduce the data throughput between sensor and the rest of the acquisition system, so that a few external resources are required in order to build the rest of the system.

The paper are organized as follows. The characterization of the detector is presented in Section II. In particular we will focus on noise characteristic, dynamic range and on time-gating performance. The application data throughput is estimated in Section III and the design of a read-out system for the reported sensor is also described. An inexpensive FPGA has been chosen to implement both the sub-nanosecond timing signal generation, needed for fast gated operation, and to manage the data acquisition. Finally, the results presented in the paper are summarized in the concluding section.

II. DETECTOR DESCRIPTION AND CHARACTERIZATION

The design of this detector is fully detailed in [3]. In this section the device architecture will be briefly summarized, as schematically shown in Fig. 2.

The detector consists of an array of 10x10 SPADs (s in Fig. 2), with a pitch of 26 μ m. Each SPAD can be individually enabled or disabled using a 100 bit memory (m) that is programmed by the user through an external driver. The SPADs share the same deep n-tub implant as previously done in [4], in order to achieve a high fill factor of 48%. The array is divided into four 5x5 sectors, where all the 25 SPADs in a block are binned to the same digital readout channel. One of these sectors is marked with an A in Fig. 2. In this respect, the sensor can be also considered as a quadrant detector. The photon counts generated by each sectors are gated separately by the gate (g). All the gates in the device are controlled by two timing signals, which can be generated by an on-chip Phase Locked Loop (PLL) or alternatively by an external device (t). The two timing signals enable in sequence, respectively, two 10-bit counters (c) collecting the SPAD pulses that are discriminated during two consecutive gating windows. The contents of all the eight counters, two for each sector, are transferred to a shift register (r) for data transmission.

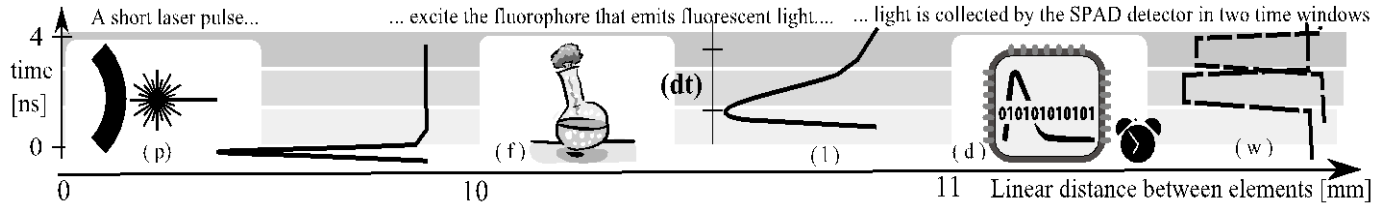


Figure 1. A picosecond Laser diode (p) is used to excite the fluorophore (f). The fluorescent light emission (l) is collected by the detector (d) through two different sampling time windows (w) to calculate the light emission decay time (dt), namely the Lifetime, of the fluorophore (f)

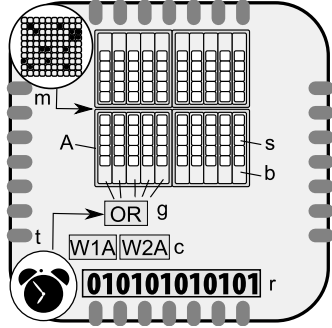


Figure 2. Chip structure, details in the text.

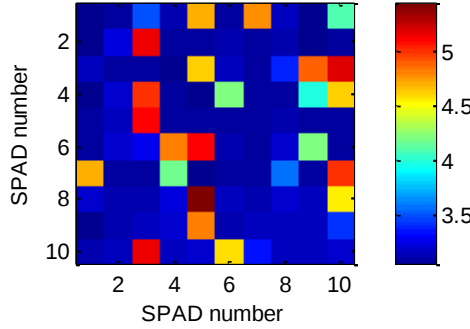


Figure 3. Dark count map at an excess bias of 4.8 V. The colored scale is logarithmic

The dark count rate (DCR, i.e. the number of counts registered in dark condition) is shown in Fig. 3. Keeping the device in the dark and at ambient temperature the memory (m) was used to enable one single SPAD at a time and to register the associated dark count rate.

The measurement was repeated at different excess bias voltage values in order to obtain the bias-dependent distribution of the dark count rate as shown in Fig. 4. In Fig. 5 the dependence of dark count rate (DCR) from the excess bias voltage can be observed for different SPADs. Three different SPADs are graphed from the noisiest to the less noisy one.

More than 70% of single SPADs have a dark count rate lower than 1 kHz at the lowest excess bias voltage and do not exceed 2 kHz at the highest one, whereas about 20% of SPADs (exact number depends on applied excess bias voltage) show dark count rates higher than 10 kHz. This happens due to random distributed defects within the SPAD active area. Total dark count rate over the SPAD array can be kept below 100 kHz in the case of switching-off noisy SPADs (up to 30% of the 10x10-SPAD array).

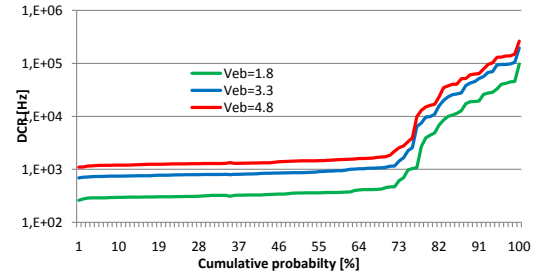


Figure 4. Dark count distribution at three different excess bias in the range from 1.8 to 4.8 V

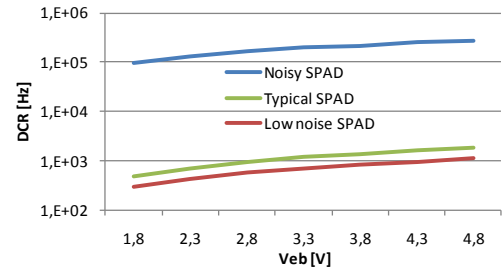


Figure 5. DCR as a function of the excess bias voltage for different SPADs

By exploiting the division of the SPAD matrix in four sectors we were able to extract information about optical cross-talk [5] between neighboring SPADs belonging to different sectors. In particular, we measured how much the count rate of a SPAD with low DCR is affected by switching on and off a neighboring noisy SPAD. The cross-talk values measured on different SPADs of the same array are visually reported in Fig. 6. The value associated with each arrow indicates the amount of increasing counting rate detectable after the enabling of the noisy neighbor. The cross-talk between lateral neighbors is between 2% and 3%, whereas for diagonal neighbors it decreases down to 0.3% - 0.5%.

A characterization of the sensor dynamic range was performed by using a wide spectrum stabilized halogen lamp and a set of neutral density filters. With this setup, optical light intensities spanning more than four orders of magnitude could be generated. The noisier SPADs of the array were disabled, so that 81 of the 100 SPADs were active during the measurement, and the total dark count rate was lower than 100 kHz. A graph showing the number of counts in the array as a function of incident optical power density is shown in Fig. 7. A total integration time of 2 ms was used in the

measurement, and the count rate was corrected for the total dead time and for the dark count rate. The sensor dynamic range, limited in the low end by the dark count rate shot noise and on the high end by sensor saturation, is about 5 orders of magnitude. The count rate reduction at high light intensities is due to the binning of different SPADs to the same counters. It is worth noting that the maximum count rate of the sensor before saturation is 500 MHz. A dynamic range exceeding 120 dB is observed with 1-second integration time.

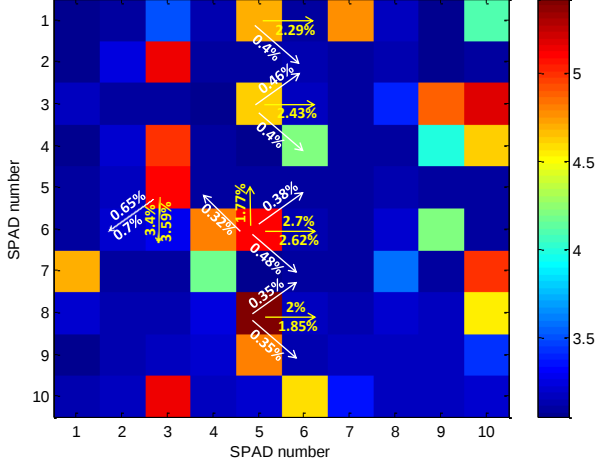


Figure 6. Optical cross-talk obtained exploiting the division of the SPAD matrix in 4 sectors

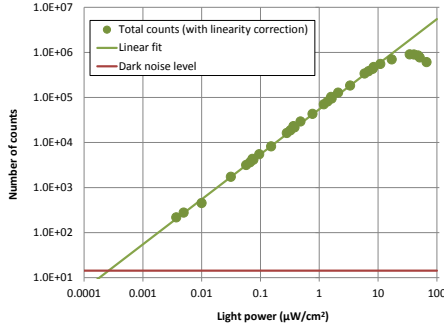


Figure 7. Sensor output as a function of optical power density with 2ms integration time

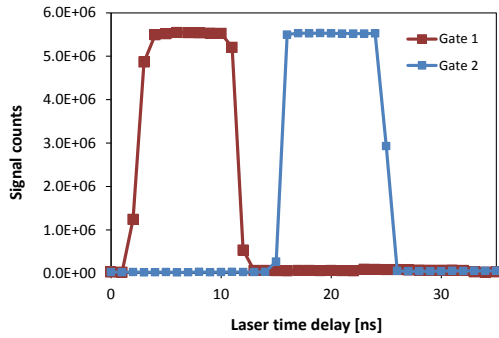


Figure 8. Sensor output as a function of laser pulse delay

A picosecond pulsed diode laser (Picoquant, $\lambda=470\text{nm}$, FWHM = 70ps) was used to characterize the gating performance of the sensor. The attenuated laser beam hit a diffuser placed in front of the sensor, while two time gates with variable time delays from the laser trigger were generated by using a two-output pulse generator (HP 8110A). The output of the two-gated counters as a function of the time delay is shown in Fig. 8, with the two gates width set to 9 ns. A sub-ns time resolution can be observed in this measurement.

Finally, a set of fluorescence lifetime measurements were performed on ZnS-ZnSe quantum-dot reference slides placed in front of the chip, exploiting the time-filtering capabilities of gated measurements. Fluorescence was excited with the same laser used in the previous experiment. A lifetime non-uniformity lower than 1% was observed among the four 5x5 quadrants with 500 kHz fluorescence counts per quadrant in the first window.

III. SYSTEM DESCRIPTION

A sketch of the implemented acquisition system is shown in Fig. 9, together with the data flow generated by the device during an experiment. In this section the volume of generated data is estimated and the architecture designed to manage the sensor data stream is described.

To perform the previously presented measurement regarding the dynamic range, the system data throughput has to be fast enough to manage the situation when all the SPADs are triggered at their maximum toggling speed. Taking into account the dead time of 200 ns, the number of SPADs binned in a sector (25 SPADs), the capacity of the counters (1023 counts) and the shift register width (80 bit), the expected data throughput is 1.2 MB/s.

Anyway this condition is quite far from a real experimental situation. Taking into account a laser frequency of 40 MHz, the maximum photon counting rate to avoid pile-up artifacts should be around 2 MHz [6]. This condition can be considered as a “worst case scenario” corresponding to the case where the total number of fluorescence light photons collected is 5% of the total number of laser pulses, a condition that is difficult to reach in an experimental setup. The expected sensor readout rate in this condition is approximately 2 KHz. In this case the driver should read the shift register every 500 μs and the total required bit rate is 160 kbps

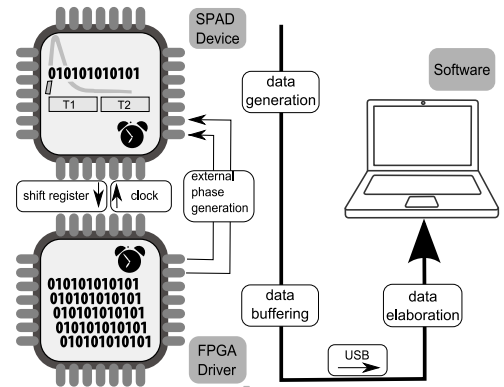


Figure 9. Schematic view of the system design

An FPGA development board provided by Opalkelly (XEM3001) [7] was chosen as data buffer between the PC and the device. Data are transferred from the FPGA driver to PC using a USB connection. Using Opalkelly libraries the maximum transfer rate is 38 MB/s, so the driver can be used to control a large number of detectors in a future configuration.

We also tested the possibility to feed the time phases to the SPAD matrix using the internal clock resources of the embedded Xilinx FPGA. This FPGA provides advanced clocking capabilities using four dedicated devices called Digital Clock Managers (DCM). The four devices are connectable in groups of two but one is used by the Opalkelly Frontpanel firmware. We considered the use of two of the three remaining DCM to generate the signal to enable the two time phases. Due to internal limitation of the Spartan 3 device and to the number of requested resources, not all the clock signals can be routed using dedicated clock buffers. Because of that an offset is expected between the imposed delay and the one obtained.

In Fig. 10 we report the measurement of the offset between two imposed phase delays (dcm1 and dcm2) and the values that were programmed. The measure was obtained using a Tektronix DPO Oscilloscope. The offset is constant at different setting, the behaviour is linear, and the measured time errors are negligible for the considered application.

IV. CONCLUSIONS

In this work we reported the characterization of a Lifetime detector realized in 0.35 μm High Voltage CMOS technology that exploits Time-gated fluorescence spectroscopy technique.

The measurement technique is performed by the detector using 10-bit gated counters. This characteristic allows for the simplification of the remaining part of the acquisition system. In particular we reported how a simple and easy to use commercial FPGA development board is a well suited (in the practical cases oversized) solution for both data buffering and external phase generation.

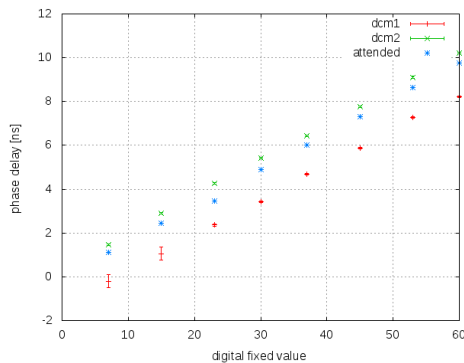


Figure 10. Measured offset between two generated phase delays (dcm1 and dcm2) and the values that were programmed. The significant time errors are the ones reported in the right side of the graph

Moreover, the architecture of this device allows switching-on/off every single SPAD independently, so that the dark count distribution can be easily built. This feature permits to find the proper number of SPADs to be switched-off in a future application as a compromise between overall detection efficiency (that decreases with reduction of number of working SPADs) and the Signal to Noise ratio (that increases with switching-off noisy SPADs).

The division of the device in sectors permits the observation of the optical crosstalk between neighboring SPADs. A value between 2% and 3% was measured for lateral neighbors, whereas for diagonal neighbors the measured value decreases to 0.3% - 0.5%. The dynamic range was measured by using a custom optical bench and the value was found to be 120 dB while the time-gating resolution was less than 1ns. A fluorescent lifetime measurement of ZnS-ZnSe Quantum-Dot reference slides was performed and the four values of calculated lifetime, one for each sector, differ by less than 1%.

The proposed Lifetime detector architecture is well designed for application as Lab-on-chip system where the constraints of the measurement scenario are single photon detection capability and on-chip data reduction. We are planning to employ a matrix of these detectors in a micro-reactor array for fluorescence markers-based bio-affinity assays.

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